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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/470,329	Applicant(s) BENNETT ET AL.
	Examiner Denise Tran	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL ACTION

1. The applicant's amendment filed 5/2/03 has been considered. Claims 1-21 are presented for examination.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-5 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376 (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli).

As per claim 1, Gilbert shows a method in multiprocessor system (e.g. figs. 1-2 and 6-8C), the method comprising:

identifying a first bus transaction that attempts to modify a shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit and preventing live-lock. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44) and preventing live-lock (e.g., col. 2, lines 43-50 and col. 3, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 7, Gilbert shows the use of a method in a multiprocessor system, the method comprising (e.g. figures 1-2 and 6-8C):

issuing a first bus transaction that attempts to modify a cache line (fig. 6, el. 50; fig. 7, el. 76; and col. 7, line 5 and col. 9, lines 48-52);

setting a status flag to indicate that a bus transaction attempting to modify the cache line is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20)

issuing a second bus transaction to read the cache line (e.g., fig. 8C, el. 112 and col. 9, lines 16-18);

retrying the second bus transaction if the status flag is set (e.g. fig. 8C, els. 114-116));

reissuing the first bus transaction that attempts to modify the cache line (e.g., fig. 8C, el. 120 and col. 11, lines 20);

granting the cache line for the reissued first bus transaction if the status flag is set for the cache line (e.g., fig. 8C, el. 122 and col. 11, lines 9-21).

Gilbert does not specifically show the use of the status flag as a bit and preventing live-lock. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44) and preventing live-lock (e.g., col. 2, lines 43-50 and col. 3, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claims 2 and 8, Gilbert teaches clearing the status flag when the reissued first bus transaction completes (e.g., fig. 8C, el. 122). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage

requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli col. 3, lines 1-3.

As per claim 4, Gilbert shows the use of clearing the status flag at periodic intervals (e.g., fig. 8C, el. 124). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 5, Gilbert shows the use of clearing the status flag at periodic intervals (e.g., fig. 8C, el. 124) and a given period of time can be any desired value (e.g., col. 11, lines 29-44). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag

(i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Gilbert does not explicitly show periodical intervals being longer than a length of time for a bus transaction to complete. "Official Notice" is taken that both the concept and advantage of having periodical intervals being longer than a length of time for a bus transaction to complete are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the periodical intervals are longer than a length of time for a bus transaction to complete because it would allow sufficient time to finish the transaction and reduce the number of retry requests, thereby improving the system performance.

4. Claims 3, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376, (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli), as applied to claims 1 and 7 above, and further in view of Donley et al., U.S. Patent No. 5,761,446 (hereinafter Donley).

As per claims 3, 6, and 9, Gilbert shows the use of clearing the status flag by a counter where the counter can be any desired value (e.g., col. 11, lines 29-44). As stated above, Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at

the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo- random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

5. Claims 10-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al., U.S. Patent No. 5,897,656, (hereinafter Vogt) in view of Gilbert et al., U.S. Patent No. 6,041,376) (hereinafter Gilbert).

As per claim 10, Vogt shows the use of a multiprocessor computer system comprising:

a plurality of processors (e.g., fig. 1, els. 112);

a resource shared by the plurality of processors (e.g., fig.1, el. 132);

at least one system bus interconnecting the shared resource and the plurality of processors (e.g., fig.1, el. 102);

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on the at least one system bus by one of the processors (e.g. figure 2, elements 208 and 210 and figure 5A, els 500 and fig. 6; and col. 25, line 54 to col. 26, line 27); and

a status indicator associated with each of the plurality of buffers (e.g. col. 26, lines 16-27; col. 28, lines 24-26), and a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried (e.g., col. 25, lines 61-64; and col. 27, lines 32-45).

Vogt does not specifically show the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource. Gilbert shows the use of a status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource (e.g., fig. 8C, el. 110; col. 9, line 63-65 and col. 11, lines 9-20; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

As per claim 11, Vogt shows the use of four processors are coupled to each one of the system buses (e.g. figure 1, elements 112a-d and additional processors interpreted as at least four; and col. 16, lines 50-57).

As per claim 12, Vogt shows the use of at least one system bus comprises two processor buses (e.g. figure 1, elements 102 and 104).

As per claim 13, Vogt shows the use of four processors coupled to each one of the two processor buses (e.g. figure 1, elements 102, 104 and 112a-d and additional processors interpreted as at least four; and col. 16, lines 50-57.

As per claim 14, Vogt shows the use of an input/output bus (e.g. figure 1, element 106).

As per claim 15, Vogt shows the use of a multiple bus, multiprocessor computer system (e.g., fig. 1, els 102, 104, and 112) comprising:

a plurality of processors (fig. 1, els. 112);

a plurality of data cache memories (e.g. fig. 1, els. 114);

a system memory shared by the plurality of processors (e.g. fig. 1, el. 132);

at least two buses interconnecting the system memory with the plurality of data cache memories and the plurality of processors (e.g. fig. 1, els. 102 and 104); and

a controller (e.g. fig. 1, el. 130) comprising:

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on one of the buses by one of the processors (e.g. fig. 2, els. 208 and 210 and fig. 5A, els. 500 and fig. 6; and col. 25, line 54 to col. 26, line 27); and

a status indicator associated with each of the plurality of buffers (e.g. col. 26, lines 16-27; col. 28, lines 24-26), and a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried (e.g., col. 25, lines 61-64; and col. 27, lines 32-45).

Vogt does not specifically show the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource. Gilbert shows the use of a status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource (e.g., fig. 8C, el. 110; col. 9, line 63-65 and col. 11, lines 9-20; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

As per claim 16, Vogt shows each one of the at least two buses is coupled to four of the processors (e.g. figure 1, elements 102, 104 and 112a-d and additional processors interpreted as at least four; and col. 16, lines 50-57).

As per claim 17, Vogt shows the use of an integrated circuit (e.g., fig. 2, el. 130 and col. 18, lines 43-46) comprising:

a bus interface to control a plurality of bus transactions (e.g. fig. 1, el. 204);

a coherency module to maintain cache coherency for a plurality of cache lines (e.g., fig. 2, el. 200); and

a buffer manager (e.g., fig. 2, el. 210) comprising,

a plurality of buffers (e.g. fig. 5A, els. 500), each one of the buffers to store information associated with one of the plurality of bus transactions received by the bus interface (e.g. fig. 5A, els. 500 and col. 26, lines 7-27); and

a plurality of status indicators where at least one of the status indicators associated with each of the buffers (e.g. fig. 5A, els. 502, 505), and one of the bus transactions attempting to modify one of the cache lines is retried (e.g., col. 25, lines 61-64; and col. 27, lines 32-45).

Vogt does not specifically show the status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried. Gilbert shows the use of status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried (e.g., fig. 8C, els. 110-122; col. 9, line 63-65 and col. 11, lines 9-24; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

As per claim 18, Vogt shows the use of the buffer manager further comprises logic to determine a type of bus transaction occurring on a bus (e.g. fig. 5A, el. 505 and col. 26, lines 24-27).

As per claim 19, Vogt shows the use of the buffer manager further comprises logic to determine if two of the bus transactions are contending for a same cache line (e.g. fig. 5B, els. 510 and col. 14, lines 10-30, col. 27, line 22 to col. 28, line 16).

As per claim 20, Vogt does not explicitly show logic to reset all of the plurality of status indicators. Gilbert shows logic to reset all of the plurality of status indicators (e.g., fig. 8C, els. 124 or 122; col. 2, lines 51-60; and col. 11, lines 9-30, where all the status flag can be reset at different times). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guarantee forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied and by limiting the amount of time that other processors are prevented from accessing the data as taught by Gilbert col. 2, line 41 to col. 3, line 8.

As per claim 21, Vogt shows the use of 64 buffers and 64 status indicators (e.g. figure 5A, els 500 and 502, 505 and col. 26, lines 15-20).

6. Applicant's arguments filed 5/2/03 have been fully considered but they are not persuasive.

7. In the remarks, the applicant's argued that the cited combination did not teach every element of amend in dependent claim 1.

The examiner disagreed with the applicant's arguments because Gilbert reference and Arimilli reference when combined teach every element of amend independent claim 1. As stated in the rejections above, Gilbert shows a method in multiprocessor system (e.g. figs. 1-2 and 6-8C), the method comprising:

identifying a first bus transaction that attempts to modify a shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit and preventing live-lock. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44) and preventing live-lock (e.g., col. 2, lines 43-50 and col. 3, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of

Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

8. In the remarks, the applicant's argued that the hold flag is for preventing nodes or processors from accessing a data line, but not for indicating that a bus transaction attempting to modify a shared resource is pending.

The examiner disagreed with the applicant's arguments because the combination of Gilbert and Arimilli references teaches all the elements of the claimed invention as stated in the rejections. In particular, Gilbert not only teach the status flag (i.e., hold flag) for preventing nodes or processors from accessing a data line, but also teaches, e.g., col. 11, lines 9-20; col. 8, line 56 to col. 9, line 20; and abstract, the status flag for indicating a bus transaction attempting to modify the shared resource is pending. According to Gilbert, when the status (i.e., hold) flag is set, it indicates the bus request transaction to the data line being pending and only the pending request is allow to access the data line (e.g., fig. 8C, els 120-122 and col. 11, lines 9-20). Gilbert also, teaches, e.g., abstract and fig. 8C, els 120-122, the status flag is clear when the request is satisfied. As seen from e.g., col. 8, line 56 to col. 9, line 20 Gilbert teaches that the request can be a write request. Therefore, Gilbert teaches status flag for indicating that a bus transaction attempting to modify a shared resource is pending.

9. In the remarks, the applicant's argued that Gilbert does not teach retrying each subsequent nonmodifying bus transaction until the status bit is cleared.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner disagreed with the applicant's arguments because the combination of Gilbert and Arimilli references teaches all the elements of the claimed invention as stated in the rejections. In particular, Gilbert, col. 11, lines 9-25, teaches when the status flag is set, the particular bus request transaction to the data line pending and the subsequent bus transactions from the other nodes for the same cache line (i.e., bus transaction after the pending request) should be retried until the status flag is clear. According to fig. 8C, Gilbert shows when the status (i.e. hold) flag is set, retrying each subsequent bus transaction (e.g., els. 112-116); and when the status flag is clear, allowing accessing data to a bus transaction (e.g., els 118). As applicant's notice (Applicant's amendment filed 5/2/03, page 9, lines 5-6) that Gilbert at col. 9, lines 14-18, teaches a bus request transaction from the other processors can be reading the data line (i.e., nonmodifying bus transaction). Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44) and preventing live-lock (e.g., col. 2, lines 43-50 and col. 3, lines 1-3). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Therefore, the combination of Gilbert and Arimilli references teaches retrying each subsequent nonmodifying bus transaction until the status bit is clear.

10. In the remarks, the applicant's argued that the Office Action did not cite any passage from Arimilli that taught a status bit.

The examiner disagreed with the applicant's arguments, as stated in the office action the combination of Gilbert and Arimilli teaches all the elements of the claimed invention, as specially a status bit. In particular, Gilbert shows a method in multiprocessor system (e.g. figs. 1-2 and 6-8C), the method comprising:

identifying a first bus transaction that attempts to modify a shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52);

setting a status flag to indicate that a bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20); and

retrying each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a bit and preventing live-lock. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44) and preventing live-lock (e.g., col. 2, lines 43-50 and col. 3, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Therefore, the combination of Gilbert and Arimilli references teaches a status bit. Also, Arimilli shows a status bit (i.e., mode bit; e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44).

11. In the remarks, the applicant's argued that Gilbert did not teach granting the cache line for the reissued first bus transaction if the status bit is set for the cache line as set forth in independent claim 7.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner disagreed with the applicant's arguments because the combination of Gilbert and Arimilli references teaches all the elements of the claimed invention as stated in the rejections. In particular, according to Gilbert, when the status (i.e., hold) flag is set, the data line being held for the first bus request transaction (e.g., fig. 8C, els. 120-122 and col. 11, lines 9-21) and the cache line is granted to the first bus request transaction when the request is retried (e.g., fig. 8C, els 120-122 and col. 11, lines 9-21). Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44) and preventing live-lock (e.g., col. 2, lines 43-50 and col. 3, lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Therefore, the combination of Gilbert and Arimilli references teaches granting the cache line for the reissued first bus transaction if the status bit is set for the cache line as set forth in independent claim 7.

12. In the remarks, the applicant's argued that Donley did not teach a status bit as claimed in dependent claims 3, 6, and 9.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner disagreed with the applicant's arguments because the combination of Gilbert, Arimilli, and Donley references teaches all the elements of the claimed invention as stated in the rejections, as specifically a status bit. In particular, Gilbert shows the use of clearing the status flag by a counter where the counter can be any desired value (e.g., col. 11, lines 29-44). Gilbert does not specifically show the use of the status flag as a bit. Arimilli shows the use of a flag as a bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo- random number (e.g.,

col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

Therefore, the combination of Gilbert, Arimilli, and Donley references teaches a status bit as claimed in dependent claims 3, 6, and 9.

13. In the remarks, the applicant's argued that Gilbert did not teach "a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried", claims 10, 15.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner disagreed with the applicant's arguments because the combination of Vogt and Gilbert references teaches the claimed limitation as stated in the rejections. In particular, Vogt shows the use of a multiple bus, multiprocessor computer system (e.g., fig. 1, els 102, 104, and 112) comprising:

a status indicator associated with each of the plurality of buffers (e.g. col. 26, lines 16-27; col. 28, lines 24-26), and a first one of the processors initiates a bus

transaction attempting to modify the shared resource and the bus transaction is retried (e.g., col. 25, lines 61-64; and col. 27, lines 32-45).

Vogt does not specifically show the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource. Gilbert shows the use of a status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource (e.g., fig. 8C, el. 110; col. 9, line 63-65 and col. 11, lines 9-20; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

In further discussion, according to Gilbert, when the status (i.e., hold) flag is set, indicating a first processor initiating a bus request transaction to the data line (e.g., fig. 8C, els. 120-122 and col. 11, lines 9-21) and the cache line is granted when the bus request transaction is retried (e.g., fig. 8C, els 120-122 and col. 11, lines 9-21). Also, Gilbert teaches the request can be a write request (e.g., col. 9, lines 48-52).

14. In the remarks, the applicant's argued that Gilbert did not teach "a plurality of status indicators to indicate that one of the bus transactions attempting to modify one of

the cache lines is retried, at least one of the status indicators associated with each one of the buffers" claim 17.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner disagreed with the applicant's arguments because the combination of Vogt and Gilbert references teaches the claimed limitation as stated in the rejections. In particular, Vogt shows the use of an integrated circuit (e.g., fig. 2, el. 130 and col. 18, lines 43-46) comprising:

a plurality of status indicators where at least one of the status indicators associated with each of the buffers (e.g. fig. 5A, els. 502, 505), and one of the bus transactions attempting to modify one of the cache lines is retried (e.g., col. 25, lines 61-64; and col. 27, lines 32-45).

Vogt does not specifically show the status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried. Gilbert shows the use of status indicators indicating that one of the bus transactions attempting to modify one of the cache lines is retried (e.g., fig. 8C, els. 110-122; col. 9, line 63-65 and col. 11, lines 9-24; and fig. 7, el. 76; col. 7, line 5 and col. 9, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of

processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col.2, lines 41-50.

In further discussion, according to Gilbert, when the status (i.e., hold) flag is set, indicating the bus request transaction is retried to the data line (e.g., fig. 8C, els. 120-122 and col. 11, lines 9-21; and col. 10, line 60 to col. 11, line 20) and the status flag is clear when the bus request transaction is retried (e.g., fig. 8C, els 120-122 and col. 11, lines 9-21). Also, Gilbert teaches the request can be a write request (e.g., col. 9, lines 48-52).

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zulian (5941967) is cited to show a retry attempts;

Bogin et al. (6502150) is cited to show a status bit.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday, and an alternate Wednesday from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7467-239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DT

Denise Tran

7/9/03

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100